LISTING OF CLAIMS:

The present listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a trench having an inner wall in a substrate;

forming an insulation film on the inner wall of the trench;

forming a conductive film in the trench on the insulation film; and

annealing the substrate for improvement of reliability of the insulation film at an annealing temperature after the step of forming the conductive film so that a damage in the insulation film is removed at the annealing temperature,

wherein the substrate is made of silicon, and

wherein the annealing temperature is higher than 1150 degrees Celsius and is equal to or less than 1200 degrees Celsius.

2. (Original) The method according to claim 1, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

3. (Cancelled)

4. (Currently Amended) The method according to claim ~~3~~ 1, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

5. (Original) The method according to claim 1,

wherein the conductive film is made of doped poly crystalline silicon, and

wherein the insulation film is made of silicon oxide and silicon nitride.

6. (Original) The method according to claim 5, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

7. (Original) The method according to claim 1,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the trench includes a sidewall and upper and lower portions,

wherein the oxide-nitride-oxide film is disposed on the sidewall of the trench, the upper oxide film is disposed on the upper portion of the trench, and the lower oxide film is disposed on the lower portion of the trench,

wherein the oxide-nitride-oxide film includes a silicon oxide film, a silicon nitride film and another silicon oxide film, and

wherein the upper and lower oxide films are made of silicon oxide.

8. (Original) The method according to claim 7, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

9. (Original) The method according to claim 1,

wherein the device includes a cell region and a gate lead wire region,

wherein the cell region includes a plurality of cells, each of which works as a transistor, and

wherein the gate lead wire region includes a gate lead wire.

10. (Original) The method according to claim 9,

wherein the transistor is an N channel type MOSFET, a P channel type MOSFET or an IGBT.

11. (Currently Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a trench having an inner wall in a substrate;

forming an insulation film on the inner wall of the trench;

forming a gate electrode in the trench on the insulation film;

implanting an impurity into the substrate with using the gate electrode as a mask after the step of forming the gate electrode;

performing a thermal diffusion process for diffusing the impurity so that a source region adjacent to the trench and disposed on a surface of the substrate is formed; and

annealing the substrate <u>for improvement of reliability of the insulation film</u> at an annealing temperature after the step of forming the conductive film so that a damage in the insulation film is removed at the annealing temperature,

wherein the substrate is made of silicon, and

wherein the annealing temperature is higher than 1150 degrees Celsius and is equal to or less than 1200 degrees Celsius.

12. (Original) The method according to claim 11,

wherein the thermal diffusion process is performed at a process temperature, and

wherein the annealing temperature in the step of annealing is higher than the process temperature in the step of performing the thermal diffusion process.

13. (Original) The method according to claim 11,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the trench includes a sidewall and upper and lower portions,

wherein the oxide-nitride-oxide film is disposed on the sidewall of the trench, the upper oxide film is disposed on the upper portion of the trench, and the lower oxide film is disposed on the lower portion of the trench,

wherein the oxide-nitride-oxide film includes a silicon oxide film, a silicon nitride film and another silicon oxide film, and

wherein the upper and lower oxide films are made of silicon oxide.

14. (Original) The method according to claim 13, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

15. (Currently Amended) The method according to claim 14,

wherein the distance between the edge of the canopy and the edge of the opening of the trench is in a range between 0.05 micrometers and 0.1 micrometers.

16. (Previously Presented) The method according to claim 11,

wherein the substrate is annealed in an inert gas atmosphere in the step of annealing.

17. (Withdrawn) A semiconductor device having a trench gate structure, comprising:

a semiconductor substrate having a trench with an inner wall disposed in the substrate;

an insulation film disposed on the inner wall of the trench;

a gate electrode disposed in the trench through the insulation film; and

a source region adjacent to the trench and disposed on a surface portion of the substrate,

wherein the insulation film does not include a damage therein.

18. (Withdrawn) The device according to claim 17,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the trench includes a sidewall and upper and lower portions,

wherein the oxide-nitride-oxide film is disposed on the sidewall of the trench, the upper oxide film is disposed on the upper portion of the trench, and the lower oxide film is disposed on the lower portion of the trench,

wherein the oxide-nitride-oxide film includes a silicon oxide film, a silicon nitride film and another silicon oxide film, and

wherein the upper and lower oxide films are made of silicon oxide.

19. (Withdrawn) The device according to claim 18,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section, and

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench.

20. (Withdrawn) The device according to claim 19,

wherein the source region is prepared in such a manner that an impurity is implanted into the substrate with using the gate electrode as a mask, and then the impurity is diffused with a thermal diffusion process,

wherein the damage in the insulation film is eliminated in such a manner that the insulation film is annealed at an annealing temperature after the gate electrode is formed, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

21. (Withdrawn) The device according to claim 20,

wherein the substrate is made of silicon, and

wherein the annealing temperature is equal to or higher than 1150°C.

22. (Withdrawn) The device according to claim 17,

wherein the gate electrode is made of doped poly crystalline silicon, and

wherein the insulation film includes a silicon oxide film and a silicon nitride film.

23. (Withdrawn) The device according to claim 17,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the trench includes an sidewall and upper and lower portions,

wherein the oxide-nitride-oxide film is disposed on a sidewall of the trench, the upper oxide film is disposed on an upper portion of the trench, and the lower oxide film is disposed on a lower portion of the trench,

wherein the oxide-nitride-oxide film includes a silicon oxide film, a silicon nitride film and another silicon oxide film, and

wherein the upper and lower oxide films are made of silicon oxide.

24. (Withdrawn) The device according to claim 17, further comprising:

a cell region and a gate lead wire region,

wherein the cell region includes a plurality of cells, each of which works as a transistor, and

wherein the gate lead wire region includes a gate lead wire.

25. (Withdrawn) The method according to claim 24,

wherein the transistor is an N channel type MOSFET, a P channel type MOSFET or an IGBT.